Claims

[c1] 1. A chip package structure, comprising:
a substrate, having an upper surface and a lower surface;
a chip, having an active surface and a back surface, wherein the active surface of the chip is mounted to the upper surface of the substrate, and the chip is electrically connected to the substrate;
a stiffener, disposed on the upper surface of the substrate and around the chip;
a first heat sink, disposed on the back surface of the chip and on the stiffener; and
a second heat sink, disposed on the lower surface of the substrate and below the chip.

[c2] 2. The package structure of claim 1, wherein the second heat sink further includes at least one fin to increase the heat dissipation efficiency.

[c3] 3. The package structure of claim 1, wherein a material of the first heat sink includes a metal.

[c4] 4. The package structure of claim 1, wherein a material of the second heat sink includes a metal.

[c5] 5. The package structure of claim 1, further comprising a plurality of bumps through which the chip is mounted on the upper surface of the substrate and electrically connected to substrate.

[c6] 6. The package structure of claim 5, further comprising an underfill material between the chip and the substrate.

[c7] 7. The package structure of claim 1, further comprising a plurality of solder balls, wherein the solder balls are disposed on the lower surface and around the second heat sink

[c8] 8. The package structure of claim 1, wherein the stiffener and the first heat sink are integrally formed as an integral single body.

[c9] 9. The package structure of claim 1, wherein an area of the second heat sink is smaller than that of the chip.

[c10] 10. A chip package structure, comprising:
a substrate, having an upper surface and a lower surface;
a chip, having an active surface and a back surface, wherein the active surface of the chip is mounted to the upper surface of the substrate, and the chip is electrically connected to the substrate;
a stiffener, disposed on the upper surface of the substrate and around the chip;

a first heat sink, disposed on the back surface of the chip and on the stiffener; and
a second heat sink, disposed on the lower surface of the substrate and below the chip, wherein a coefficient of thermal expansion of the second heat sink is the same as that of the substrate.

[c11] 11. The package structure of claim 10, wherein the second heat sink further includes at least one fin to increase the heat dissipation efficiency.

[c12] 12. The package structure of claim 10, wherein a material of the first heat sink includes a metal.

[c13] 13. The package structure of claim 10, wherein a material of the second heat sink includes a metal.

[c14] 14. The package structure of claim 10, further comprising a plurality of bumps through which the chip is mounted on the upper surface of the substrate and electrically connected to substrate.

[c15] 15. The package structure of claim 14, further comprising an underfill material between the chip and the substrate.

[c16] 16. The package structure of claim 10, further comprising a plurality of solder balls, wherein the solder

balls are disposed on the lower surface and around the second heat sink

[c17] 17. The package structure of claim 10, wherein the stiffener and the first heat sink are integrally formed as an integral single body.

[c18] 18. The package structure of claim 10, wherein the lower surface of the substrate further has a central area and the second heat sink is attached to the central area.